In the Claims:

Please amend claims 25, 28, 34 and 37. Please cancel claims 1-24 and 43-70. The claims are as follows:

1-24 (Canceled)

25. (Currently Amended) An integrated circuit, comprising:

a test pin, a first test clock pin, a second test clock pin, a third test clock pin, a functional clock pin, a scan-in pin, a scan-out pin and an enable pin;

a test controller having a test input connected to said test pin, a first test clock input connected to said first test clock pin, a functional clock input connected to said functional clock pin, a first control output and a second control output;

a clock splitter having a first clock input connected to said second test clock pin, a second clock input connected to said functional clock pin, a first control input connected to said first control output of said test controller, a second control input connected to said second control output and of said controller, an enable input connected to said enable pin, a ZB clock output and a ZC clock output; and

an LSSD scan chain comprised of serially connected latches, a first stage of each latch having a[[n]] first data input, a second data input and a C clock input connected to said ZC clock output of said clock splitter, an A CLK input connected to said third test clock pin, a second stage of each latch having a data output and a B clock input connected to said ZB clock output of said clock splitter, a data output of a previous latch connected to a first input pin of an immediately subsequent latch, a first data input of a first latch of said LSSD scan chain

connected to said scan-in pin and a data output pin of a last scan chain latch of said scan chain connected to said scan-out pin.

26. (Original) The circuit of claim 25, wherein said test controller includes:

an output of a first latch connected to an input of a second latch, an output of said second latch connected to an input of a third latch, said second latch having a feedback connection to an input of said first latch and said third latch having feedback connections to said first and said second latches;

combinational logic coupled to said first, second and third latches, said combinational logic coupled to said test pin, said first test clock pin and said functional clock pin;

said first latch coupled through said combinational logic to said second control output; and

said feedback connection of said second latch further coupled through said combinational logic to said first control output.

27. (Original) The circuit of claim 25, further including:

additional clock splitters connected to said test controller, some or all of said additional clock splitters connected to corresponding additional scan chains.

28. (Currently Amended) The circuit of claim 25, wherein:

said test controller is responsive to generate a first control signal of one cycle of said functional clock signal in duration on said first control pin and to generate a second control signal having a duration of two cycles of said functional clock signal on said second control

output upon a transition from a first state to a second state of a test signal applied to said test pin, said first control signal starting a half a cycle of said functional clock cycle after the start of said second control signal; and

said clock splitter is responsive to generate a first B clock pulse on said ZB clock output, followed by a C clock pulse on said ZC clock output, followed by a second B clock pulse on said ZB clock output, said B and C clock pulses at the same frequency as said functional clock signal, based on said first and second control signals.

29. (Original) The circuit of claim 28, wherein:

(a) if said functional clock is in a high state prior to said test signal transitioning to a high state then, within a sequence of five consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, said second control signal is generated on a first edge and terminated on a fifth edge and said first control signal is generated on a second edge and terminated a fourth edge of said sequence of five consecutive edges of said functional clock signal; and

(b) if said functional clock is in a low state prior to said test signal transitioning to a high state, then within a sequence of four consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, said second control signal is generated on a first edge and terminated on a fourth edge and said first control signal is generated on a first edge and terminated on a third edge of said sequence of four consecutive edges of said functional clock signal.

30. (Original) The circuit of claim 28, wherein:

(a) if said functional clock is in a high state prior to said test signal transitioning to a high state, then within a given sequence of five consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, said first B clock pulse is generated on a second edge and terminated on a third edge, said C clock pulse is generated on said third edge and terminated on a fourth edge, and said second B clock pulse is generated on said fourth edge and terminated on a fifth edge of said sequence of five consecutive edges of said functional clock signal; and

(b) if said functional clock is in a low state prior to said test signal transitioning to a high state, then within a given sequence of four consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, said first B clock pulse is generated on a first edge and terminated on a second edge, said C clock pulse is generated on said second edge and terminated on a third edge, and said second B clock pulse is generated on said third edge and terminated on a fourth edge of said sequence of five consecutive edges of said functional clock signal.

31. (Original) The circuit of claim 28, wherein said first and second B clock pulses cause data in said first stages of said latches to be captured by said second stages of said latches and said C clock pulse causes data states on said data pin to be latched by said first stages of said latches.

32. (Original) The circuit of claim 28, wherein:

said functional clock signal has a higher frequency than that of a B test clock signal applied to said first test clock pin and that of a C test clock signal applied to said second test clock pin; and

when said test signal is in said second state, data previously entered into first stages of said latches while said B test clock signal was applied to said first test clock pin and while said C clock test signal was applied to second test clock pin is prevented from being replaced until after a data transfer from said first stages of said latches to second stages of said latches while said functional clock signal is applied to said first and second test clock pins instead of said B test clock and C test clock signals.

33. (Original) The circuit of claim 28, wherein said test controller is further adapted to generate no more than one pulse of said first control signal and one pulse of said second control signal without a transition of said test signal from said first state to a second state intervening.

34. (Currently Amended) A method of testing an integrated circuit, comprising:

providing a test pin, a first test clock pin, a second test clock pin, a third clock pin, a functional clock pin, a scan-in pin, a scan-out pin and an enable pin;

providing a test controller having a test input connected to said test pin, a first test clock input connected to said first test clock pin, a functional clock input connected to said functional clock pin, a first control output and a second control output;

providing a clock splitter having a first clock input connected to said second test clock pin, a second clock input connected to said functional clock pin, a first control input connected to said first control output of said test controller, a second control input connected to said second control output and of said controller, an enable input connected to said enable pin, a ZB clock output and a ZC clock output; and

providing an LSSD scan chain comprised of serially connected latches, a first stage of each latch having a[[n]] first data input, a second data input and a C clock input connected to said ZC clock output of said clock splitter, an A clock input connected to said third test clock pin, a second stage of each latch having a data output and a B clock input connected to said ZB clock output of said clock splitter, a data output of a previous latch connected to a first input pin of an immediately subsequent latch, a first data input of a first latch of said LSSD scan chain connected to said scan-in pin and a data output pin of a last scan chain latch of said scan chain connected to said scan-out pin.

35. (Original) The method of claim 34, wherein said test controller includes:

an output of a first latch connected to an input of a second latch, an output of said second latch connected to an input of a third latch, said second latch having a feedback connection to an input of said first latch and said third latch having feedback connections to said first and said second latches;

combinational logic coupled to said first, second and third latches, said combinational logic coupled to said test pin, said first test clock pin and said functional clock pin;

said first latch coupled through said combinational logic to said second control output; and

said feedback connection of said second latch further coupled through said combinational logic to said first control output.

36. (Original) The method of claim 34, further including:

connecting additional clock splitters to said test controller, some or all of said additional clock splitters connected to corresponding additional scan chains.

37. (Currently Amended) The method of claim 34, further including:

said test controller generating a first control signal of one cycle of said functional clock signal in duration on said first control pin and generating a second control signal having a duration of two cycles of said functional clock signal on said second control output upon a transition from a first state to a second state of a test signal applied to said test pin, said first control signal starting a half a cycle of said functional clock cycle after the start of said second control signal; and

said clock splitter generating a first B clock pulse on said ZB clock output, followed by a C clock pulse on said ZC clock output, followed by a second B clock pulse on said ZB clock output, said B and C clock pulses at the same frequency as said functional clock signal, based on said first and second control signals..

38. (Original) The method of claim 37, further including:

(a) if said functional clock is in a high state prior to said test signal transitioning to a high state then, within a sequence of five consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, generating said second control signal on a first edge, terminating said second control signal on a fifth edge, generating said first control signal on a second edge and terminating said first control signal a fourth edge of said sequence of five consecutive edges of said functional clock signal; and

(b) if said functional clock is in a low state prior to said test signal transitioning to a high state, then within a sequence of four consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, generating said second control signal on a first edge, terminating said second control signal on a fourth edge, generating said first control signal on a first edge and terminating said first control signal on a third edge of said sequence of four consecutive edges of said functional clock signal.

39. (Original) The method of claim 37, further including:

(a) if said functional clock is in a high state prior to said test signal transitioning to a high state, then within a given sequence of five consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, generating said first B clock pulse on a second edge and terminating said first B clock pulse on a third edge, generating said C clock pulse on said third edge and terminating said C clock pulse on a fourth edge, and generating said second B clock pulse on said fourth edge and terminating said second B clock pulse on a fifth edge of said sequence of five consecutive edges of said functional clock signal; and

(b) if said functional clock is in a low state prior to said test signal transitioning to a high state, then within a given sequence of four consecutive edges of said functional clock signal each edge defining a change of state of said functional clock signal, generating said first B clock pulse on a first edge, and terminating said first B clock pulse on a second edge, generating said C clock pulse on said second edge and terminating said C clock pulse on a third edge, and generating said second B clock pulse on said third edge and terminating said second B clock pulse on a fourth edge of said sequence of five consecutive edges of said functional clock signal.

40. (Original) The method of claim 37, further including:

capturing data said second stages of said latches in response to said first and second B clock pulses; and

latching data states on said data pins of said first stages of said latches in response to said C clock pulse.

41. (Original) The method of claim 37, wherein:

said functional clock signal has a higher frequency than that of a B test clock signal applied to said first test clock pin and that of a C test clock signal applied to said second test clock pin; and

when said test signal is in said second state, data previously entered into first stages of said latches while said B test clock signal was applied to said first test clock pin and while said C clock test signal was applied to second test clock pin is prevented from being replaced until after a data transfer from said first stages of said latches to second stages of said latches while said functional clock signal is applied to said first and second test clock pins instead of said B test clock and C test clock signals.

42. (Original) The method of claim 37, further including said test controller generating no more than one pulse of said first control signal and one pulse of said second control signal without a transition of said test signal from said first state to a second state intervening.

43-70 (Canceled)